(19) **Publication country** Japan Patent Office (JP)
(12) **Kind of official gazette** Open patent official report (A)
(11) **Publication No.** JP,2003-257173,A (P2003-257173A)
(43) **Date of Publication** September 12, Heisei 15 (2003. 9.12)
(54) **Title of the Invention** The readout circuitry of a semiconductor memory
(51) **The 7th edition of International Patent Classification**

G11C 11/14
11/15
H01L 27/105
43/08

FI

G11C 11/14 Z
11/15
H01L 43/08 Z
27/10 447

Request for Examination Un-asking.
The number of claims 24
Mode of Application OL
Number of Pages 20
(21) **Application number** Application for patent 2002-56810 (P2002-56810)
(22) **Filing date** March 4, Heisei 14 (2002. 3.4)
(71) **Applicant**
Identification Number 000004237
Name Nippon Electric Co., Ltd.
Address 5-7-1, Shiba, Minato-ku, Tokyo
(72) **Inventor(s)**
Name Sakimura **
Address 5-7-1, Shiba, Minato-ku, Tokyo Inside of Nippon Electric Co., Ltd.
(72) **Inventor(s)**
Name Honda ****
Address 5-7-1, Shiba, Minato-ku, Tokyo Inside of Nippon Electric Co., Ltd.
(72) **Inventor(s)**
Name Cedar forest Naohiko
Address 5-7-1, Shiba, Minato-ku, Tokyo Inside of Nippon Electric Co., Ltd.
(74) **Attorney**
Identification Number 100096253
Patent Attorney
Name Omi Yusuke
Theme code (reference)

5F083

F term (reference)

5F083 FZ10 LA10

(57) **Abstract**
Technical problem It is a low power in small area, and read-out of a high speed is possible, and the readout circuitry of MRAM of a self-reference method is offered.
Means for Solution By read-out of the 1st, the current inputted from the selection cel 13 is changed into the pulse of the frequency in inverse proportion to the current value by pre amplifier 3 and VCO4, and the pulse number within fixed time amount counts with a counter 5, and is memorized by the read-out value register 6. Next, a selection cel is written in either of two storage conditions, and read-out of the 2nd is performed. The storage condition of a selection cel is distinguished by comparing the counted value of the counter in read-out

of the 2nd, and the counted value at the time of read-out of the 1st memorized by the read-out value register with the reference value memorized by the reference-value register 7. The integral capacitor and reference pulse generation means of a current which were the need conventionally are made unnecessary using VCO, it is a low power in small area, and read-out of a high speed is possible.

Claim(s)

Claim 1 It is the readout circuitry of the 1st storage condition that resistance is small, and the semiconductor memory, with which a memory cell array consists of memory cells which have relatively two storage conditions with the 2nd storage condition that resistance is large relatively. The pre amplifier which detects the current inputted from the selection cel chosen among said memory cells, and carries out magnification conversion at an electrical potential difference, The voltage controlled oscillator oscillated on the frequency proportional to the output voltage of said pre amplifier, The counter which counts the pulse number outputted from said voltage controlled oscillator, and a counted value storage means to memorize the output value of said counter, The readout circuitry of the semiconductor memory characterized by having a judgment means for the output value of said counter and said counted value storage means to be inputted and to judge the storage condition of said selection cel.

Claim 2 The readout circuitry of the semiconductor memory according to claim 1 characterized by the output in fixed time amount of said counter being the digital value which changes in monotone to the resistance of said selection cel.

Claim 3 The readout circuitry of the semiconductor memory according to claim 1 or 2 characterized by to perform the 2nd read-out and ** which are performed after read-out of the 1st, the writing which writes either said 1st storage condition or the 2nd storage condition in said selection cel after said read-out of the 1st, and said writing, and to perform the judgment of the storage condition of said selection cel by said judgment means after selection of said selection cel.

Claim 4 It has a reference-value storage means by which the reference value D used for the stored data judging of said selection cel is stored. Output-value C2nd of said counter **output-value C1st of said counter at the time of said read-out of the 1st is stored in said counted value storage means, and** at the time of said read-out of the 2nd, The readout circuitry of the semiconductor memory according to claim 3 characterized by judging the storage condition of said selection cel by said judgment means using output-value C1st of said counted value storage means, and the output value D of said reference-value storage means.

Claim 5 When the storage condition of the memory cell of the arbitration in said memory cell array is read When the value outputted from said counter when it is in C (1) and the 2nd storage condition about the value outputted from said counter when the memory cell of said arbitration is in the 1st storage condition is set to C (2), The readout circuitry of the semiconductor memory according to claim 4 characterized by being set as the value of the range with which said reference value D fills 0<D<C **|C(1)-** (2) |.

Claim 6 When said selection cel is written in the 1st storage condition at the time of said writing Said judgment means is the following inequality. C2 nd-C1 st-D<0 If it becomes 1st storage condition C2 nd-C1 st-D>=0 If it becomes It is based on the 2nd storage condition. The readout circuitry of the semiconductor memory according to claim 4 or 5 characterized by judging the storage condition at the time of read-out **said selection cel** of the 1st.

Claim 7 When said selection cel is written in the 2nd storage condition at the time of said writing Said judgment means is the following inequality. C2 nd-C1 st+D<0 If it becomes 1st storage condition C2 nd-C1 st+D>=0 If it becomes It is based on the 2nd storage condition. The readout circuitry of the semiconductor memory according to claim 4 or 5 characterized by judging the storage condition at the time of read-out **said selection cel** of the 1st.

Claim 8 The readout circuitry of the semiconductor memory according to claim 3 characterized by storing output-value C1st of said counter at the time of said read-out of the 1st in said counted value storage means, and judging the storage condition of said selection cel by said judgment means using output-value C2nd of said counter at the time of said read-out of the 2nd, and output-value C1st of said counted value storage means.

Claim 9 The readout circuitry of the semiconductor memory according to claim 8 with which said pre amplifier is characterized by operating in the gain or/and the operating point which are different in the time of said read-out of the 1st and said read-out of the 2nd.

Claim 10 When it reads using the memory cell of the arbitration in said memory cell array In the gain or/and the operating point at the time of read-out **said pre amplifier** of the 1st The oscillation frequency of said voltage controlled oscillator in case said memory cell is in the 1st storage condition f1st(1), In the gain **make the oscillation frequency of said voltage controlled oscillator in the case of being in the 2nd storage condition into f1st(2), and** at the time of read-out **said pre amplifier** of the 2nd, or/and the operating point When the oscillation frequency of said voltage controlled oscillator in the case of being in f2nd(1) and the 2nd storage condition about the oscillation frequency of said voltage controlled oscillator in case said memory cell is in the 1st storage condition is made into f2nd(2), When the 1st storage condition and the 2nd storage condition are written in said selection cel at the time of said writing, it is the next relational-expression f1st(2) <f2nd(1)

<f1st (1), respectively.
f1st(2)<f2nd(2)<f1st(1)
********** -- the readout circuitry of the semiconductor memory according to claim 9 characterized by adjusting the gain or/and the operating point of said pre amplifier at the time of read-out of the 1st and read-out of the 2nd like.

Claim 11 The readout circuitry of the semiconductor memory according to claim 3 or 8 characterized by the read-out time amount of said read-out of the 1st differing from the read-out time amount of said read-out of the 2nd.

Claim 12 Said judgment means is the following inequality C2 nd-C1st<0. If it becomes The 1st storage condition C2 nd-C1st>=0 If it becomes Readout circuitry of a semiconductor memory given in either of claims 8-11 characterized by being based on the 2nd storage condition and judging the storage condition at the time of read-out **said selection cel** of the 1st.

Claim 13 It is the readout circuitry of the 1st storage condition that resistance is small, and the semiconductor memory, with which a memory cell array consists of memory cells which have relatively two storage conditions with the 2nd storage condition that resistance is large relatively. The pre amplifier which detects the current inputted from the selection cel chosen among said memory cells, and carries out magnification conversion at an electrical potential difference, The readout circuitry of the semiconductor memory characterized by having an electrical-potential-difference comparison means for an electrical-potential-difference storage means to memorize the output voltage of said pre amplifier, and the output voltage of said pre amplifier and the output voltage of said electrical-potential-difference storage means to be inputted, and to compare both electrical potential differences.

Claim 14 It is the readout circuitry of the 1st storage condition that resistance is small, and the semiconductor memory, with which a memory cell array consists of memory cells which have relatively two storage conditions with the 2nd storage condition that resistance is large relatively. The pre amplifier which detects the current inputted from the selection cel chosen among said memory cells, and carries out magnification conversion at an electrical potential difference, The 1st switching means which turns the output of said pre amplifier on and off, and the inverter connected to the latter part of the 1st switching means through the capacitor, The readout circuitry of the semiconductor memory characterized by having the latch circuit connected to the latter part of said inverter, and the 2nd switching means connected to said inverter at juxtaposition.

Claim 15 It is the readout circuitry of the 1st storage condition that resistance is small, and the semiconductor memory, with which a memory cell array consists of memory cells which have relatively two storage conditions with the 2nd storage condition that resistance is large relatively. An integral means to integrate with the current inputted from the selection cel chosen among said memory cells, The readout circuitry of a semiconductor memory which has an electrical-potential-difference comparison means for an electrical-potential-difference storage means to memorize the electrical potential difference outputted from said integral means, and the output voltage of said integral means and the output voltage of said storage means to be inputted, and to compare both electrical potential differences.

Claim 16 The writing which writes either said 1st storage condition or the 2nd storage condition in said selection cel after read-out of the 1st and said read-out of the 1st after selection of said selection cel, The readout circuitry of a semiconductor memory given in either of claims 13-15 characterized by performing the 2nd read-out and ** which are performed after said writing, and the judgment of the storage condition of said selection cel being performed by said electrical-potential-difference comparison means or said latch circuit.

Claim 17 Said pre amplifier is the readout circuitry of the semiconductor memory according to claim 16 characterized by operating in the gain or/and the operating point which it is at said said 1st read-out actuation and read-out actuation time of ** a 2nd, and are different.

Claim 18 The readout circuitry of the semiconductor memory according to claim 16 characterized by said integral means having a time constant which is different in the time of said read-out of the 1st and said read-out of the 2nd.

Claim 19 The readout circuitry of the semiconductor memory according to claim 16 characterized by the reset time at the time of said read-out of the 1st differing from the reset time at the time of said read-out of the 2nd.

Claim 20 The gain or/and the operating point of said pre amplifier at the time of read-out of the 1st when it reads using the memory cell of the arbitration in said memory cell array, In the time constant or the reset time of said integral means, said pre amplifier in case said memory cell is in the 1st storage condition, or the output voltage of said integral means Or V1st(1), Said pre amplifier in the case of being in the 2nd storage condition or output voltage of said integral means is made into V1st(2). The gain or/and the operating point of said pre amplifier at the time of read-out of the 2nd, In the time constant or the reset time of said integral means, said pre amplifier in case said memory cell is in the 1st storage condition, or the output voltage of said integral means Or V2nd(1), When said pre amplifier in the case of being in the 2nd storage condition or output voltage of said integral means is made into V2nd(2), When the 1st storage condition and the 2nd storage condition are written in said selection cel at the time of said writing, it is the next relational-expression V1st(2) <V2nd(1) <V1st (1), respectively.
V1st(2)<V2nd(2)<V1st(1)

********** -- the readout circuitry of a semiconductor memory given in either of claims 17-19 characterized by adjusting the time constant or the reset time of the gain of said pre amplifier at the time of read-out of the 1st and read-out of the 2nd or/and the operating point, or said integral means like.
Claim 21 If said pre amplifier at the time of read-out of the 2nd or output voltage of said integral means is set to V1st and V2nd, respectively at the time of read-out of the 1st Said electrical-potential-difference comparison means is the following inequality V2 nd-V1st<0. If it becomes The 1st storage condition V2 nd-V1st>=0 If it becomes It is based on the 2nd storage condition. The readout circuitry of a semiconductor memory given in either of claims 16-20 characterized by judging the storage condition at the time of read-out **said selection cel** of the 1st.
Claim 22 The readout circuitry of a semiconductor memory given in either of claims 16, 17, 20, and 21 which said 1st and 2nd switching means are closed at the time of read-out of the 1st, and Kaisei of closing and said 2nd switching means is carried out for said 1st switching means at the time of read-out of the 2nd, and are characterized by latching the output voltage of said inverter at the time of read-out of the 2nd to said latch circuit.
Claim 23 The readout circuitry of a semiconductor memory given in either of claims 3-22 to which the storage condition at the time of read-out **said selection cel** of the 1st is characterized by being written in said selection cel after said judgment when the storage condition at the time of read-out **said said judged selection cel** of the 1st differs from the storage condition written in at the time of said writing.
Claim 24 The readout circuitry of a semiconductor memory given in either of claims 1-23 characterized by said memory cell having the tunnel magnetic resistance element.

Detailed Description of the Invention
0001
Field of the Invention This invention relates to the readout circuitry of a semiconductor memory, especially the readout circuitry of a semiconductor memory which has a memory cell containing a tunnel magnetic resistance element.
0002
Description of the Prior Art Drawing 21 shows the structure and the principle of a tunnel magnetic resistance element (henceforth "TMR"). As shown in drawing 21 (a), TMR610 has the two-layer magnetic layers 653 and 654 formed up and down on both sides of the insulator layer 652 and the insulator layer 652, and both the thickness of 10-20A and magnetic layers 653 and 654 of the thickness of an insulator layer 652 is about 50A. One magnetic layer 653 in magnetic layers 653 and 654 is called a pin layer, and the sense of the magnetization does not change with impression of the field in the operating range of TMR, but is being fixed to the sense at the time of manufacture. Another magnetic layer 654 is a layer from which it is called a free layer and the sense of the magnetization changes with impression of the field in the operating range of TMR. Drawing 21 (a) shows the condition that the free layer 654 is magnetized to the sense contrary to the pin layer 653. When electric field are impressed between the free layer 654 and the pin layer 653 at this time, the tunnel current which flows an insulator layer 652 is small, and TMR610 shows high resistance. In this condition, if the field beyond the threshold from which the free layer 654 starts flux reversal is impressed to the sense of magnetization of the pin layer 653, and parallel TMR610, magnetization of the free layer 654 will be reversed. Drawing 21 (b) shows the condition of having carried out flux reversal. If electric field are impressed between the free layer 654 and the pin layer 653 at this time, the tunnel current which flows an insulator layer 652 will become large, and the resistance of TMR610 will decrease.
0003 The semiconductor memory (henceforth "MRAM") which assigns two resistance conditions of TMR, for example, the high resistance condition of drawing 21 (a), to a storage condition "1", assigns the low resistance condition of drawing 21 (b) to a storage condition "0", and is memorized is known by using TMR as a memory cell using this resistance change of TMR. Drawing 22 is a top view **(a)** and sectional view **(b)** for explaining actuation of the memory cell of MRAM. As shown in drawing 22 (a), TMR710 is inserted, and it wires so that the upper and lower sides and a word line 711 and the bit line 712 may cross at right angles mutually, respectively. The sense of the arrow head of a continuous line is the direction where a current flows. As shown in drawing 22 (b), TMR710 changes more with the insulator layer 752, the pin layer 753 and the free layer 754 which sandwich an insulator layer 752, the antiferromagnetic substance layer 755 formed in the bottom of the pin layer 753, and the cap layer 756. the antiferromagnetic substance layer 755 -- the direction of magnetization of the pin layer 753 -- fixing -- the direction of magnetization of the free layer 754 -- reversal -- it is formed in order to make it easy, therefore TMR710 has spin bulb mold structure. The cap layer 756 has protected the antiferromagnetic substance layer 755 and the free layer 754. The writing of data, i.e., the flux reversal of the free layer 754, is performed by passing a current to a word line 711 and a bit line 712. When the current of a word line 711 and a bit line 712 is flowing to the sense as shown in drawing 22 (a), a field occurs in the free layer 754 rightward from the space left according to the current which flows from under the space of drawing 22 (a) to a bit line 712 above according to the current which flows from Ampere's law to a word line 711. Therefore, in the free layer 754, the synthetic field which goes to the upper right from the space lower left

works. Here, if the direction of the current which flows to a word line 711 and a bit line 712 is reversed, the sense of the synthetic field committed in the free layer 754 will be reversed, and it will go to the lower left from the space upper right. Thereby, magnetization of the free layer 754 is reversed. Therefore, the writing of data is performed by controlling the direction of the current which flows to a word line 711 and a bit line 712.

0004 Read-out of data measures the current and the both-ends electrical potential difference of TMR which flow to TMR, and can be realized by measuring the resistance of TMR indirectly. the time of setting the resistance of R and TMR of "1" storage condition to (R+deltaR) for the resistance of TMR of "0" storage condition here -- MR ratio =deltaR/Rx -- MR ratio defined by 100 (%) serves as an index showing the margin of TMR of operation, and usually has 10 - 30% of value.

0005 As one example of MRAM which used such TMR for the memory cell, the structure which has arranged the reference cel other than a memory cell in a memory cell array on the U.S. Pat. No. 6205073 specifications is indicated. The resistance of a reference cel is immobilization and has the middle value of the resistance of "0" storage condition of TMR and the resistance of "1" storage condition which constitute a memory cell. Read-out of stored data carries out magnification conversion of the current which flows in the selected memory cell and a reference cel at an electrical potential difference, and is performed by comparing the size of the electrical potential difference. If the electrical potential difference obtained from a memory cell is smaller than the electrical potential difference obtained from a reference cel, the storage condition of a memory cell is "1", and if large, the storage condition of a memory cell is "0."

0006 However, TMR used for the storage element of MRAM consists of the both very thin insulator layer and magnetic layer as mentioned above. The tunnel current which passes an insulator layer here in applied-voltage regularity, therefore the resistance of TMR change exponentially to the thickness. For example, 20 - 30% of resistance dispersion will arise only by only one atomic layer (2-3A) becoming thick, or the thickness of an insulator layer becoming thin. However, it is most difficult to generate the uniform insulator layer whose dispersion of thickness is 1 atomic-layer level. This resistance dispersion of TMR becomes more remarkable, as the area of TMR becomes small. therefore, in MRAM by the above-mentioned conventional technique Although the electrical potential difference obtained from a memory cell becomes larger than the electrical potential difference obtained from a reference cel although the storage condition of a memory cell is "1", or the storage condition of a memory cell is "0" The problem to which the electrical potential difference obtained from a memory cell becomes smaller than the electrical potential difference obtained from a reference cel occurs, and this becomes the big factor which worsens the cel yield.

0007 In order to solve the problem by dispersion in such resistance of TMR, MRAM from which a storage condition is read by the self-reference method is indicated without using a reference cel for a U.S. Pat. No. 6188615 specification. Drawing 23 is the circuit block diagram of MRAM by this advanced technology. As shown in drawing 23 , MRAM by this advanced technology consists of a memory cell array 802 and a readout circuitry 801. The memory cell which consists of only one TMR810 which exists in each intersection of the word line 811 and bit line 812 which intersect each other perpendicularly is arranged in the shape of a matrix, and the memory cell array 802 is formed. At the time of read-out, only the selection cel chosen by X selector and Y selector is connected with a readout circuitry 801, and only the current which flows a selection cel with the electrical potential difference impressed among the both ends of a selection cel is inputted into a readout circuitry 801. The readout circuitry 801 consists of the integral means 830, electrical-potential-difference comparison means 808A, a counter 805, presetting register 807A, a judgment means 808, a reference pulse generation means 834, and a control circuit 809. The integral means 830 has the charge amp 833 and the integral capacitor 832.

0008 With the integral means 830, on an electrical potential difference, magnification conversion is carried out and the current which flows in a selection cel finds the integral. A readout circuitry 801 measures the resistance of a selection cel indirectly by measuring the time amount Tint until the integral electrical potential difference Vint with which it integrated with the integral means 830 becomes equal to reference voltage Vr. Electrical-potential-difference comparison means 808A is always comparing the size of Vint and Vr, and during the period which is Vint<=Vr, when a counter 805 counts the pulse number of the reference pulse of the fixed period generated with the reference pulse generation means 834, it is changed into the digital value to which Tint is proportional to the counted pulse number.

0009 Drawing 24 is an explanatory view of operation for explaining actuation of the readout circuitry of drawing 23 . the -- one -- read-out -- setting -- selection -- a cel -- TMR -- "-- zero -- " -- storage -- a condition -- it is -- a case -- a counter -- 805 -- counting -- having -- a pulse number -- c -- one -- st -- (-- zero --) -- "-- one -- " -- storage -- a condition -- it is -- a case -- a counter -- 805 -- counting -- having -- a pulse number -- c -- one -- st -- (-- one --) -- being few . Next, pulse number c2nd counts with a counter 805 until this selection cel is written in "0" or "1" storage condition and serves as Vint=Vr like read-out of the 1st in read-out of the 2nd. In drawing 24 , it is written in "0" storage condition. From the number of counts counted by read-out of the 1st and the 2nd, the storage condition of the selection cel at the time of read-out of the 1st is determined.

0010 Drawing 25 is a flow chart for explaining actuation of the readout circuitry of drawing 23 . one memory cell chooses -- having (step S801) -- counted value CNT=d / 2 are loaded to a counter 805 (step S802). Here, it is d= **c(0)-c (1)**, and when TMR is in "0" storage condition and "1" storage condition, c (0) and c (1) are the numbers of counts which will be counted with a counter 805 by the time the integral electrical potential

difference Vint becomes equal to reference voltage Vr, and are measured using **in a memory array (for example, the memory cell of arbitration)** , respectively. In this case, d takes a negative value. Next, read-out of the 1st is performed (step S803). The counted value CNT of a counter 805 becomes the sum of counter value c1st and d/2 which were obtained by read-out of the 1st. Next, after **- (c1 st+d/2)** is memorized by presetting register 807A, the contents are reloaded to a counter 805 (step S804). Next, "0" storage condition is written in a selection cel (step S805). Next, read-out of the 2nd is performed (step S806). The counted value CNT of a counter 805 serves as the sum **c2nd- (c1 st+d/2)** of counter value c2nd obtained by read-out of the 2nd, and the already loaded counted value **- (c1 st+d/2)**. Next, the positive/negative of CNT is judged by the judgment means 808 (step S807). If CNT is forward, it will judge that the storage condition at the time of read-out **a selection cel** of the 1st is "0" (step S808), and read-out actuation will end it. If CNT is negative, it will be judged with the storage condition at the time of read-out **a selection cel** of the 1st being "1" (step S809). When judged with the storage condition of a selection cel being "1", if needed, "1" storage condition is re-written in a selection cel (step S810), and read-out actuation is completed. Thus, by reading twice, the storage condition of the cel in MRAM is performed based on a self-reference method, without using a reference cel. Since the difference of own "0" storage condition of a memory cell and "1" storage condition is used for the judgment of the storage condition of a memory cell by the above self-reference method, it is possible to mitigate the effect by resistance dispersion between memory cells.

0011

Problem(s) to be Solved by the Invention In the Prior art mentioned above, after choosing a cel, always load d/2 which is a constant to a counter, or make counted value of a counter into a reverse sign after read-out of the 1st, a presetting register is made to memorize, the procedure of reloading the contents to a counter is needed, and fixed time amount is spent. What is necessary is to prepare separately the register which memorizes the 1st read-out result, and just to make the 1st read-out result memorize, in order to avoid this until the 2nd read-out actuation is completed to this register. d/2 of values are contained by the presetting register. However, in that case, the register circuit for several bits is required, and circuit area increases. Furthermore, circuit area becomes large with the integral capacitor used for an integral means. resistance:100k **for example,** of one TMR -- between the both ends of ohm and TMR when voltage drop:0.5V, Vr:0.5V, and reset-time:1microsec, 10pF is needed as a capacity of an integral capacitor. In order for an integrated circuit to realize capacity of 10pF, 40x40-micrometer two or more fields are required using gate capacitance. Moreover, as a reference pulse generation means, although PLL (Phase-Locked Loop) is usually used, it becomes the big cause by which this also increases circuit area and power consumption.

0012 the non-volatile semiconductor memory with which this invention was made in view of these technical problems, and the purpose used the tunnel magnetic resistance element -- setting -- a facet -- it is a low power by the product, and read-out of a high speed is possible, and it is offering the readout circuitry by which degradation of the yield by dispersion in the resistance of TMR is prevented.

0013

Means for Solving the Problem In order to attain the above-mentioned purpose, according to this invention, relatively The 1st storage condition that resistance is small, It is the readout circuitry of the semiconductor memory with which a memory cell array consists of memory cells which have relatively two storage conditions with the 2nd storage condition that resistance is large. The pre amplifier which detects the current inputted from the selection cel chosen among said memory cells, and carries out magnification conversion at an electrical potential difference, The voltage controlled oscillator oscillated on the frequency proportional to the output voltage of said pre amplifier, Readout-circuitry ** characterized by having the counter which counts the pulse number outputted from said voltage controlled oscillator, at least one storage means, and a judgment means to judge the storage condition of said selection cel is offered.

0014 In order to attain the above-mentioned purpose, according to this invention, relatively Moreover, the 1st storage condition that resistance is small, It is the readout circuitry of the semiconductor memory with which a memory cell array consists of memory cells which have relatively two storage conditions with the 2nd storage condition that resistance is large. The pre amplifier which detects the current inputted from the selection cel chosen among said memory cells, and carries out magnification conversion at an electrical potential difference, Readout-circuitry ** characterized by having a storage means to memorize the output voltage of said pre amplifier, and an electrical-potential-difference comparison means to input the output voltage of said storage means is offered.

0015 In order to attain the above-mentioned purpose, according to this invention, relatively Moreover, the 1st storage condition that resistance is small, It is the readout circuitry of the semiconductor memory with which a memory cell array consists of memory cells which have relatively two storage conditions with the 2nd storage condition that resistance is large. The pre amplifier which detects the current inputted from the selection cel chosen among said memory cells, and carries out magnification conversion at an electrical potential difference, The 1st switching means which turns the output of said pre amplifier on and off, and the inverter connected to the latter part of the 1st switching means through the capacitor, Readout-circuitry ** of the semiconductor memory characterized by having the latch circuit connected to the latter part of said inverter and the 2nd switching means connected to said inverter at juxtaposition is offered.

0016 In order to attain the above-mentioned purpose, according to this invention, relatively Moreover, the 1st

storage condition that resistance is small, It is the readout circuitry of the semiconductor memory with which a memory cell array consists of memory cells which have relatively two storage conditions with the 2nd storage condition that resistance is large. An integral means to integrate with the current inputted from the selection cel chosen among said memory cells, Readout-circuitry ** which has an electrical-potential-difference comparison means to input an electrical-potential-difference storage means to memorize the electrical potential difference outputted from said integral means, and the output voltage of said integral means and the output voltage of said storage means is offered. And said memory cell has the tunnel magnetic resistance element preferably.

0017

Embodiment of the Invention Next, the gestalt of operation of this invention is explained to a detail with reference to a drawing.

Gestalt of the 1st operation Drawing 1 is the circuit block diagram of MRAM used for the gestalt of operation of the 1st of this invention. As shown in drawing 1 , MRAM used for the gestalt of this operation has the memory cell array 2 and the readout circuitry 1. The memory cell array 2 is a cross point cel array in which the memory cell which consists of only one TMR10 which exists in each intersection of the word line 11 and bit line 12 which intersect perpendicularly mutually and suit is arranged in the shape of a matrix, and is formed. Although only every three word lines and bit lines are shown, respectively since a plot is easy, generally the word line of several 100 - 1000 numbers and a bit line exist. At the time of read-out, a memory cell is chosen by giving a line address to the X selector 14 and giving the train address to the Y selector 15. Selection word line 11a connected to TMR10a of the selected memory cell 13 is connected to the 1st power source V1, and the subdevice-bit line 12a is connected with the input terminal of a readout circuitry. The non-choosing word line and non-subdevice-bit line by which others are not chosen are connected with the 2nd power source V2. The input terminal electrical potential difference of a readout circuitry is always made into electrical potential differences **power source / V2 / 2nd** . At this time, among the both ends of TMR10a of the selection cel 13, the electrical potential difference of the difference of the 1st power source V1 and the 2nd power source V2 is impressed, and only the current which flows to TMR10a is inputted into a readout circuitry 1. The pre amplifier 3 changed while a readout circuitry 1 amplifies the current which flows TMR of a selection cel on an electrical potential difference, VCO4 oscillated on the frequency proportional to the output voltage of pre amplifier 3 (Voltage Controlled Oscillator), The read-out value register 6 which stores in a fixed period of arbitration the output value of the counter 5 which counts the oscillation pulse number of VCO4, and a counter 5, It has a judgment means 8 to judge the storage condition memorized by the selection cel from the output value of the reference-value register 7 which stores the criterion value beforehand, two registers 6 and 7, and a counter 5, and the control circuit 9 which controls actuation of this readout circuitry 1. The criterion value D stored in the reference-value register 7 has the value |C(0)-C 0<D< (1) | Becoming. Here, C (0) and C (1) are counted value outputted from a counter 5, respectively, when TMR of a memory cell is in "0" storage condition and "1" storage condition. C (0) and C (1) are calculated as counted value of the counter 5 obtained when the memory cell of the arbitration in a memory cell array is changed into "0" storage condition and "1" storage condition, respectively and the memory cell is read. In addition, "0" storage condition and "1" storage condition mean the condition that the direction **layer / a pin layer and / free** of magnetization is parallel and anti-parallel mutually, through the gestalt of all operations, respectively.

0018 As shown in drawing 2 (a), pre amplifier 3 outputs the electrical potential difference which is proportional to the resistance of TMR of a memory cell with a negative inclination. R (0) and R (1) are resistance in case TMR of a memory cell is in "0" storage condition and "1" storage condition, respectively, and V (0) and V (1) are the output voltage of the pre amplifier 3 in case the resistance of TMR of a memory cell is R (0) and R (1), respectively. Output voltage is adjusted by adjusting the gain of pre amplifier 3. Moreover, as shown in drawing 2 (b), VCO4 is oscillated on the frequency proportional to the output voltage of pre amplifier 3. f (0) and f (1) are the oscillation frequencies of VCO4 in case the output voltage of pre amplifier 3 is V (0) and V (1), respectively. An oscillation frequency is adjusted by adjusting the gain of VCO4. Therefore, from drawing 2 (a) and drawing 2 (b), VCO4 is oscillated on the frequency which is proportional to the resistance of TMR of a memory cell with a negative inclination, as shown in drawing 2 (c). Oscillation frequency **in the margin of operation and "1" storage condition of VCO** f (1) and frequency deltaf of a difference with oscillation frequency **in "0" storage condition** f (0) can be adjusted by the gain of the input-output behavioral characteristics of pre amplifier 3, the gain of VCO4, etc. In addition, it is also possible to form a circuit so that the oscillation frequency of VCO may be proportional to the resistance of TMR of a memory cell with a forward inclination. Furthermore, between the oscillation frequency of VCO, and the resistance of TMR of a memory cell, perfect proportionality did not necessarily need to be realized and the relation which changes in monotone should just be realized.

0019 Actuation of the readout circuitry 1 of the gestalt of this operation is explained below using drawing 3 , referring to drawing 1 . Drawing 3 is an explanatory view of operation for explaining actuation of a readout circuitry 1. First, after the memory cell of arbitration is chosen, read-out **the memory cell** of the 1st is started. Read-out of the 1st transforms into an electrical potential difference the current which flows TMR of a selection cel by the pre amplifier 3 of drawing 1 as mentioned above, generates the pulse of the oscillation frequency which is proportional to the output voltage of pre amplifier 3 by VCO4, and is performed by counting the pulse

number within fixed time amount of the acquired pulse with a counter 5. Counted value C1st outputted from a counter 5 is stored in the read-out value register 6. And the counted value of a counter 5 is reset by 0. Next, after writing in so that a selection cel may be in "0" storage condition, the 2nd read-out actuation is started. Read-out of the 2nd is performed like read-out of the 1st. The read-out time amount of read-out of the 2nd is set up equally to the read-out time amount of read-out of the 1st. Counted value outputted from a counter 5 at this time is set to C2nd. The judgment means 8 judges the storage condition of the selection memory cell at the time of read-out of the 1st based on a degree type.

C2 nd-C1 st-D<0 If it becomes "0" storage condition C2 nd-C1 st-D>=0 If it becomes "1" storage condition When judged with the storage condition of the selection memory cell at the time of read-out of the 1st being in "1" storage condition by the judgment means 8 It writes in so that a selection cel may take "1" storage condition after termination of the 2nd read-out actuation if needed, and read-out actuation is ended.

0020 After the writing of "1" storage condition instead of "0" storage condition is performed in a selection cel after read-out of the 1st, the 2nd read-out actuation may be started. In this case, the judgment means 8 judges the storage condition of the selection memory cell at the time of read-out of the 1st based on a degree type.

C2 nd-C1 st+D>=0 If it becomes "1" storage condition C2 nd-C1 st+D<0 If it becomes "0" storage condition When judged with the storage condition of the selection memory cell at the time of read-out of the 1st being in "0" storage condition by the judgment means 8 It writes in so that a selection cel may take "0" storage condition after termination of the 2nd read-out actuation if needed, and read-out actuation is ended.

0021 Drawing 4 is the circuit diagram of the pre amplifier 3 of drawing 1 . This pre amplifier circuit has the function which carries out magnification conversion of the current which flows in a selection cel at an electrical potential difference, maintaining at the same electrical potential difference V2 as the 2nd power source the electrical potential difference of the input terminal connected with the subdevice-bit line in a memory cell array. The electrical-potential-difference range changed is set up in the input voltage range of VCO4 of drawing 1 . In drawing 4 , the source terminal of a transistor M1 is connected with a subdevice-bit line, and bias voltage Vb is inputted into the gate of a transistor M1 so that the electrical potential difference may be set to V2. Here, Vb is Vb**V2+Vt (Vt: threshold electrical potential difference of a transistor M1). At this time, the current Is which flows between the drain-sources of a transistor M1 becomes equal to the current which flows to TMR of a selection cel, and is given by the degree type.

Is=(V1-V2)/R (1

Here, R is the resistance of TMR. The transistor M3 and the transistor M4 form current Miller circuit, therefore the current Is equal to (1) type flows between the drain-sources of a transistor M4. On the other hand, the current Ir which flows to resistance Rref1 flows between the drain-sources of a transistor M8 by two current Miller circuits formed with a transistor M5, a transistor M6 and a transistor M7, and a transistor M8. The resistance of resistance Rref1 is set up so that the current which flows between the drain-sources of a transistor M8 may become almost equal to the current value given by (1) formula. That is, the resistance of resistance Rref1 is set up so that the operating point of pre amplifier may be adjusted according to the resistance of TMR. Here, the output voltage VPA 1 of pre amplifier is expressed with the following formulas.

VPA1=IsxRM8 -- here, RM8 is resistance between the drain-sources of a transistor M8. Thus, the current Is which flows in a selection cel is transformed into an electrical potential difference, it is enlarging resistance RM 8 between the drain-sources of a transistor M8, and the electrical potential difference is amplified.

0022 Drawing 5 is the circuit diagram of VCO4 of drawing 1 . This circuit is a VCO circuit of a common ring oscillator mold, and has the oscillation loop formation which consists of the delay cel 20 of odd level. The output voltage VPA 1 of pre amplifier is inputted into the gate of a transistor M11 as input voltage Vvcoin of VCO, and Current Iv flows between the drain-sources of a transistor M11. The transistor M12, the transistor M13 and the transistor M14, and the transistor M15 form two current Miller circuits, and a current value passes the current of Iv in each delay cel. Since Current Iv changes, therefore the time constant of each delay cel 20 also changes in proportion to input voltage Vvcoin, the oscillation frequency of VCO changes. Here, if input voltage Vvcoin turns into below the threshold electrical potential difference of a transistor M11, a current will not flow to transistors M11-M15, and the oscillation of VCO will stop. It is "high" about enable signal vcoena. By carrying out, it operates so that a transistor M16 will be in switch-on and the gate voltage of a transistor M15 may not turn into below a threshold electrical potential difference, and quenching of VCO is prevented. Moreover, if enable signal vcoena is set to "low", a transistor M17 will be in switch-on, the gate voltage of a transistor M15 will be compulsorily lowered to below a threshold electrical potential difference, and the oscillation of VCO will be stopped. Since the output swing of each delay cel is minute, it is amplified to the electrical potential difference of a logic level with the differential amplifier 21, and outputs an output Vvcoout.

0023 Drawing 6 is the TMR resistance-oscillation frequency characteristics acquired by the SPICE simulation using the VCO circuit 4 shown in the pre amplifier circuit 3 shown in drawing 4 , and drawing 5 . By changing the resistance of the resistance Rref1 of pre amplifier 3, adjustment of the margin of TMR resistance of operation or oscillation delta-frequency deltaf is possible. up to the memory cell whose resistance of TMR is 50-150kohm when referred to as Rref1=100kohm -- read-out -- possible -- MR ratio -- if it is =10%, oscillation delta-frequency deltaf will be set to about 100MHz. If the 1st aforementioned read-out time amount T1 and 2nd read-out time amount T2 are set to 1microsec, if the difference of the counted value of "1" storage

condition and "0" storage condition becomes about 100 and it is made about into D= 50, it can perform the judgment with "1" storage condition and "0" storage condition easily.

0024 As mentioned above, digitization is easily realizable by using VCO. Furthermore, since VCO has the integral function on the phase shaft, it can eliminate sneak current and alternating current-noise current like the integral means 830 of the conventional technique shown in drawing 23 . Moreover, since the integral means 830 and the reference pulse generation means 834 which are used by the readout circuitry 801 of the conventional technique shown in drawing 23 become unnecessary, reduction of circuit area or power consumption can be aimed at. Furthermore, since the procedure of loading d/2 to a counter, or making counted value of a counter into a reverse sign after read-out of the 1st, making a presetting register memorizing, and reloading the contents to a counter is not needed, read-out of a high speed is possible. Moreover, as for the readout circuitry 1 by the gestalt of this operation, since VCO is a circuit served in digital one on an electrical-potential-difference shaft, a circuit highly precise on an electrical-potential-difference shaft makes low-battery actuation unnecessary possible. Furthermore, by producing using a detailed process, it can oscillate on a still higher frequency and VCO is advantageous to detailed-izing of a device.

0025 Gestalt of the 2nd operation Drawing 7 is the circuit block diagram of the readout circuitry of the gestalt of operation of the 2nd of this invention. As shown in drawing 7 , the readout circuitry 101 of the gestalt of this operation Gain control pre amplifier 103A which carries out magnification conversion of the current which flows a selection cel at an electrical potential difference, and can control conversion gain, VCO104 oscillated on the frequency proportional to the output voltage of gain control pre amplifier 103A, The counter 105 which counts the pulse number of the oscillation pulse of VCO104 at a fixed period of arbitration, A judgment means 108 to judge the storage condition memorized by the selection cel from the output value of the read-out value register 106 which stores the output value of a counter 105, the read-out value register 106, and a counter 105, It has the control circuit 109 which controls actuation of this readout circuitry 101. In drawing 7 , the reference mark with a single equal figure is given to the component which has the same or, same function as drawing 1 the bottom, and the detailed explanation is omitted.

0026 The memory cell array of the same configuration as the memory cell array 2 of the gestalt of the 1st operation is connected to the input of gain control pre amplifier 103A. 102 expresses with one memory cell the memory cell array connected to the input of gain control pre amplifier 103A. Two N-channel metal oxide semiconductor FET expresses X selector and Y selector, respectively, and the end of a cel is connected to the 1st power source V1 at the input of gain control pre amplifier 103A currently held at the electrical potential difference with the other end equal to the 2nd power source V2, respectively by making two N-channel metal oxide semiconductor FET into switch-on. With the gestalt of this operation, the 1st power source V1 is touch-down potential.

0027 Drawing 8 shows how the oscillation frequency of VCO changes to the resistance of TMR of a memory cell like drawing 2 in the case of the gestalt of the 1st operation (c). In drawing 8 , Curve A shows change of the oscillation frequency of VCO obtained when the gain of gain control pre amplifier 103A is set as a certain value, and Curve B shows change of the oscillation frequency of VCO obtained when the gain of gain control pre amplifier 103A is lowered a little rather than the case of Curve A, or and.

0028 Also in the gestalt of this operation, read-out actuation based on a self-reference method by two read-out by read-out of the 1st and read-out of the 2nd is performed like the gestalt of the 1st operation. In read-out of the 1st, the gain of gain control pre amplifier 103A which gives the curve A of drawing 8 is used, and the gain of gain control pre amplifier 103A which gives the curve B of drawing 8 is used in read-out of the 2nd. In gain A1st of gain control pre amplifier 103A used for read-out of the 1st here Oscillation frequency f1st(0) of VCO in case TMR is in "0" storage condition, In gain A2nd of oscillation frequency f1st(1) of VCO in the case of being in "1" storage condition, and gain control pre amplifier 103A used for read-out of the 2nd Gain A1st and gain A2nd are adjusted so that the following relational expression may be realized between oscillation frequency f2nd(0) and **s of VCO in case TMR is in "0" storage condition.

f1st(1)<f2nd(0)<f1st(0)

0029 Next, actuation of the readout circuitry of drawing 7 is explained using the flow chart of drawing 9 .

S101: A cel is chosen.

S102: The counted value of a counter 105 is set as 0.

S103: Read-out of the 1st is performed. After output-value C1st of a counter 105 is stored in the read-out value register 106, the counted value of a counter 105 is set as 0.

S104: Write "0" storage condition in a selection cel.

S105: Read-out of the 2nd is performed. The counted value of a counter 105 is C2nd.

S106: The value of H=C2 nd-C1st is calculated with the judgment means 108.

S107: With the judgment means 108, it is judged whether H is a forward value or 0.

S108: If H is a forward value, the storage condition at the time of read-out **a selection cel** of the 1st will be judged to be "1."

S109: If needed, "1" storage condition is re-written in a selection cel, and read-out actuation is completed.

S110: If H is not a forward value, the storage condition at the time of read-out **a selection cel** of the 1st will be judged to be "0", and read-out actuation will be completed.

It is the same as that of the gestalt of the 1st operation that the 1st read-out time amount and the 2nd read-

out time amount are equal.
0030 In addition, it is also possible after read-out a **selection cel** of the 1st to write in "1" storage condition instead of writing in "0" storage condition. In this case, the direction of gain A2nd of gain control pre amplifier 103A in the 2nd writing is set up more greatly than gain A1st of gain control pre amplifier 103A in the 1st writing. f1 **and** -- st (0) and f1 -- the oscillation frequency f2 of VCO in case TMR is in "1" storage condition in gain A2nd of st (1) and gain control pre amplifier 103A used for read-out of the 2nd -- gain A1st and gain A2nd are adjusted so that the following relational expression may be realized between nd (1) and **.
f1st(1)<f2nd(1)<f1st(0)
It is judged with the judgment means 108 like the case where "0" storage condition is written in after read-out a **selection cel** of the 1st whether H=C2 nd-C1st is forward, and if D is forward If "1" and D of the storage condition at the time of read-out a **selection cel** of the 1st are not forward, the storage condition at the time of read-out a **selection cel** of the 1st will be judged to be "0."
0031 Drawing 10 is the circuit diagram of gain control pre amplifier 103A of drawing 7 . In drawing 10 , the reference mark with a single equal figure is given to the component which has the same or, same function as drawing 4 the bottom, and the detailed explanation is omitted. This gain control pre amplifier circuit maintaining at the same electrical potential difference V2 as the 2nd power source the electrical potential difference of the input terminal connected with the subdevice-bit line in a memory cell array, it has the function which carries out magnification conversion of the current which flows in a selection cel at an electrical potential difference, and can still change that gain or/and operating point. The electrical-potential-difference range changed is set up in the input voltage range of VCO104 of drawing 7 . The principle of operation of gain control pre amplifier 103A is the same as that of the pre amplifier 3 of drawing 4 , and it almost, and output voltage VPA 2 is given by the degree type.
The gain and the operating point of gain control pre amplifier 103A change by adjusting VPA2=IsxRM108, therefore the resistance RM 108 between the drain-sources of M108. In drawing 10 , the value of RM108 is adjusted by preparing the criteria resistance connected to M108 in two steps, and changing them. That is, in the time of read-out of the 1st, M109 is made into switch-on, M110 is made into non-switch-on, and resistance connected to M108 is set to (Rref2+deltaRref2). Resistance which makes M109 non-switch-on, makes M110 switch-on at the time of read-out of the 2nd, and is connected to M108 is set to Rref2.
0032 In the gain control pre amplifier circuit of drawing 10 , drawing 11 shows the currents IM108 and IM104 which flow to transistors M108 and M104, when the electrical potential difference of 0-Vdd is impressed to the outputting point. Those intersections are the stable operating points of gain control pre amplifier 103A. When as for Intersection A the storage condition of a selection cel is "1", the storage condition of a selection cel is "0" in read-out of the 1st Intersection B and the storage condition of a selection cel of Intersection C is "0" in read-out of the 2nd in read-out of the 1st, it corresponds, respectively. In read-out of the 2nd, Intersection D corresponds, when the storage condition of a selection cel is "1", but when a selection cel is written in "0" storage condition after read-out of the 1st, Intersection D is a point of being meaningless.
0033 When the electrical potential difference corresponding to Intersections A, B, and C is made into V1st(1) V1st(0) V2nd(0), respectively, Rref2 and delta Rref2 are chosen so that it may become V1st(1) <V2nd(0) <V1st(0). Theoretically, as for deltaRref2/Rref2 ratio, it is desirable to carry out to about **of MR ratio** 1/2. Thus, by determining the value of Rref2 and delta Rref2, the TMR resistance-VCO oscillation frequency characteristics with which are satisfied of a formula (12) as shown in drawing 9 are acquired. Although the above is the case where a selection cel is written in "0" storage condition after read-out of the 1st When a selection cel is written in "1" storage condition after read-out of the 1st What is necessary is to make M109 into non-switch-on, to make M110 into switch-on, to make M109 into switch-on, to make M110 into non-switch-on at the time of read-out of the 2nd, and for the same procedure as **** just to determine the value of Rref2 and delta Rref2 in the time of read-out of the 1st. At this time, it considers as V1st(1) <V2nd(1) <V1st(0).
0034 As explained above, in the gestalt of the 1st operation, the required reference-value register can be deleted by transforming into an electrical potential difference the current which flows in a selection cel by different gain at the time of read-out of the 1st and read-out of the 2nd. Moreover, in the judgment by the judgment means 108, since it is possible to judge without introducing the criterion value in the gestalt of the 1st operation etc., the circuit scale of a judgment means is also reducible.
0035 Gestalt of the 3rd operation Drawing 12 is the circuit diagram of the readout circuitry of the gestalt of operation of the 3rd of this invention. As shown in drawing 12 , the readout circuitry 201 of the gestalt of this operation The pre amplifier 203 which carries out magnification conversion of the current which flows a selection cel at an electrical potential difference, and VCO204 oscillated on the frequency proportional to the output voltage of pre amplifier 203, The counter 205 which counts the pulse number of the oscillation pulse of VCO204, and the read-out value register 206 which stores the output value of a counter 205, It has a judgment means 208 to judge the storage condition memorized by the selection cel from the output value of the read-out value register 206 and a counter 205, and the control circuit 209 which controls actuation of this readout circuitry 201. In drawing 12 , the reference mark with a single equal figure is given to the component which has the same or, same function as drawing 1 the bottom, and the detailed explanation is omitted.
0036 The memory cell array 202 of the same configuration as the memory cell array of the gestalt of the 1st operation and the gestalt of the 2nd operation is connected to the input of gain control pre amplifier 103A. The

pre amplifier 3 of drawing 4 and the pre amplifier of the same configuration are used for pre amplifier 203, VCO4 of drawing 5 and VCO of the same configuration are used for it at VCO204, and initiation/halt of the oscillation are controlled by enable signal vcoena (not shown). In the gestalt of this operation, the 1st read-out time amount T1 is set up for a long time than the 2nd read-out time amount T2. Here, when referred to as T1=T2+deltaT, as for deltaT/T2 ratio, it is desirable to carry out to about **of MR ratio** 1/2.

0037 As shown in drawing 13 , also in the gestalt of this operation, read-out actuation based on a self-reference method by two read-out by read-out of the 1st and read-out of the 2nd is performed. The pulse number read by the counter like the gestalt of the 1st operation by drawing 13 in read-out in the 1st read-out time amount T1 has more direction in case the storage condition of a selection cel is "0" than the case where the storage condition of a selection cel is "1." In read-out **in / in the pulse number read when the memory cell read in read-out of the 2nd is in "0" storage condition here / the 1st read-out time amount T1** The read-out time amount T2 of read-out of the 2nd is set up so that it may become the middle value of the pulse number read when a selection cel is in "0" storage condition, and the pulse number read when a selection cel is in "1" storage condition.

0038 Read-out actuation is performed as follows. First, the memory cell of arbitration is chosen and counted value C1st counts to a counter 205 by read-out actuation of the 1st of the memory cell. Counted value C1st is stored in the read-out value register 206, and the counted value of a counter 205 is reset by 0. Next, after writing in "0" storage condition, 2nd read-out actuation is performed and counted value C2nd counts a selection cel to a counter 205. The judgment means 208 judges the storage condition of the selection memory cell at the time of read-out of the 1st based on the judgment formula given by the degree type.

C2 nd-C1st<0 If it becomes "0" storage condition C2 nd-C1st>=0 If it becomes When judged with the storage condition of the selection memory cell at the time of read-out of "1" storage condition 1st being "1", the rewrite of "1" is performed in a selection cel and read-out actuation is ended.

0039 In read-out **in / in the pulse number read when the memory cell read in read-out of the 2nd is in "1" storage condition / the 1st read-out time amount T1** The read-out time amount T2 of read-out of the 2nd may be set up so that it may become the middle value of the pulse number read when a selection cel is in "0" storage condition, and the pulse number read when a selection cel is in "1" storage condition. In this case, it is set to T1<T2. "1" storage condition is written in after read-out **a selection cel** of the 1st. The judgment means 208 judges the storage condition of the selection memory cell at the time of read-out of the 1st based on an above-mentioned judgment type.

0040 As explained above, by lengthening 2nd read-out time amount shorter than the 1st read-out time amount, in the readout circuitry 1 of the gestalt of the 1st operation, the required reference-value register becomes unnecessary, and the scale of a judgment means can also be reduced.

0041 Gestalt of the 4th operation Drawing 14 is the circuit diagram of the readout circuitry of the gestalt of operation of the 4th of this invention. As shown in drawing 14 , the readout circuitry 301 of the gestalt of this operation has electrical-potential-difference comparison means 308A which compares the size of the output voltage of gain-control pre-amplifier 303A which carries out magnification conversion of the current which flows a selection cel at an electrical potential difference, and can control conversion gain, electrical-potential-difference storage means 306A which memorizes the output voltage of gain-control pre-amplifier 303A, and electrical-potential-difference storage means 306A and gain-control pre-amplifier 303A, and the control circuit 309 which control a readout circuitry 301. In drawing 14 , the reference mark with a single equal figure is given to the component which has the same or, same function as drawing 7 the bottom, and the detailed explanation is omitted. The memory cell array 302 of the same configuration as the memory cell array of the gestalt of the 1st - the 3rd operation is connected to the input of gain control pre amplifier 303A.

0042 Also in the gestalt of this operation, read-out actuation based on a self-reference method by two read-out by read-out of the 1st and read-out of the 2nd is performed. Electrical-potential-difference storage means 306A of drawing 14 is memorized until the 2nd read-out actuation ends the output voltage of gain control pre amplifier 303A outputted at the time of the 1st read-out actuation. Gain control pre amplifier 303A has the function to change gain or the operating point in the time of read-out of the 1st and read-out of the 2nd, like the case of the gestalt of the 2nd operation.

0043 Drawing 15 shows how the output voltage of gain control pre amplifier 303A changes to the resistance of TMR of a memory cell. In drawing 15 , Curves A and B are the TMR resistance-output voltage properties of gain control pre amplifier 303A obtained in the gain of gain control pre amplifier 303A in read-out of the 1st and read-out of the 2nd, respectively. The direction of the gain of gain control pre amplifier 303A in read-out of the 1st is set up more greatly than the gain of gain control pre amplifier 303A in read-out of the 2nd. In the gain of gain control pre amplifier 303A used for read-out of the 1st here Output voltage V1st(0) of gain control pre amplifier 303A in case TMR is in "0" storage condition, In output voltage V1st(1) of gain control pre amplifier 303A in the case of being in "1" storage condition, and the gain of gain control pre amplifier 303A used for read-out of the 2nd The gain at the time of read-out of the 2nd is adjusted at the time of read-out of the 1st so that the following relational expression may be realized between output voltage V2nd(0) and **s of gain control pre amplifier 303A in case TMR is in "0" storage condition.

V1st(1)<V2nd(0)<V1st(0)

0044 Drawing 16 is an explanatory view of operation for explaining actuation of the readout circuitry 301 of

drawing 14 . Like the gestalt of the 1st operation, and the gestalt of the 2nd operation, after performing read-out of the 1st to a selection cel, it writes in "0" storage condition, and subsequently, read-out of the 2nd is performed and read-out actuation is performed. Electrical-potential-difference comparison means 308A of drawing 14 compares the size of the output voltage of electrical-potential-difference storage means 306A which has memorized the output voltage of gain control pre amplifier 303A at the time of read-out of the 1st, and the output voltage of gain control pre amplifier 303A at the time of read-out of the 2nd, and judges the storage condition at the time of read-out **a selection cel** of the 1st. Since the gain at the time of read-out of the 2nd is adjusted as mentioned above at the time of read-out of the 1st, if output voltage of gain control pre amplifier 303A in read-out of the 1st and read-out of the 2nd is set to V1st and V2nd, respectively, the following judgment type will be materialized clearly.
V2 nd-V1st<0 If it becomes "0" storage condition V2 nd-V1st>=0 If it becomes The thing which is in "1" storage condition and for which not "0" storage condition but "1" storage condition is written in after read-out of the 1st like the gestalt of the 2nd operation and the gestalt of the 3rd operation is also possible. In that case, at the time of read-out **gain control pre amplifier 303A** of the 1st, the gain at the time of read-out of the 2nd is chosen so that the conditions of V1st(1) <V2nd(1) <V1st(0) may be satisfied. The storage condition at the time of read-out **a selection cel** of the 1st is performed based on an above-mentioned judgment type.
0045 Gestalt of the 5th operation Drawing 17 (a) is the circuit diagram showing the important section of the readout circuitry of the gestalt of operation of the 5th of this invention. Although the circuit shown in drawing 17 (a) is a circuit which achieves the function of electrical-potential-difference storage means 306A of the readout circuitry of drawing 14 , and electrical-potential-difference comparison means 308A and it is not illustrated, also in the readout circuitry of the gestalt of this operation, gain control pre amplifier 303A shown in drawing 14 and a control circuit 309 are formed. The switch S1, Capacitor C, Inverter INV, and latch circuit LT are connected to the serial toward the outgoing end of a readout circuitry from the outgoing end of gain control pre amplifier, and the switch S2 is connected to Inverter INV at juxtaposition. And closing motion of switches S1 and S2 and latch actuation of latch circuit LT are performed by the control circuit by which the illustration abbreviation was carried out. Drawing 17 (b) is an explanatory view of operation for explaining actuation of drawing 17 (a), and the storage condition of the selection cel at the time of read-out of the 1st is "1", and it is written after read-out of the 1st supposing the case where the storage condition of a selection cel is written in "0." At both the times of read-out of the 1st, SUITCHI S1 and S2 is set to ON, and the value of the potentials Va and Vb of the both ends of Inverter INV becomes equal mutually. The potential of the inverter INV of Capacitor C and the terminal by the side of reverse is equal to output voltage V1st(1) of the gain control pre amplifier of the preceding paragraph. Next, after a selection cel is written in "0" storage condition, read-out of the 2nd is performed. In the time of read-out of the 2nd, SUITCHI S1 is set to ON and S2 is set to OFF. At this time, the terminal potential by the side of the gain control pre amplifier of Capacitor C rises to output voltage V2nd(0) of gain control pre amplifier. When it does so, only **V2nd(0)-V1st(1)** goes up, the input potential of Inverter INV also sways to a forward side, the output of an inverter serves as "Low", and this output is latched to a latch circuit. If read-out of the 2nd is performed after a selection cel is written in "0" storage condition when the storage condition of the selection cel at the time of read-out of the 1st is "0", as for the input potential of Inverter INV, only **V2nd(0)-V1st(0)** will sway to a negative side, and the output of an inverter will serve as "High." Thereby, the storage condition at the time of read-out **a selection cel** of the 1st is distinguished. In the gestalt of this operation, and the gestalt of the 4th operation, a limit special to the read-out time amount does not have read-out of the 1st and read-out of the 2nd.
0046 As mentioned above, in the readout circuitry of the gestalt of the 4th and the 5th operation, it has memorized to the electrical-potential-difference storage means or the capacitor by making the 1st read-out result into an electrical potential difference or the amount of charges. Therefore, the counter for changing into digital value, a reference pulse generation means, and since digital circuits, such as a register and a judgment means, can also be deleted further, a circuit scale can be sharply made smaller than the conventional readout circuitry. Moreover, since it is not necessary to count a pulse number, a read-out rate can also be shortened.
0047 Gestalt of the 6th operation Drawing 18 is the circuit diagram of the readout circuitry of the gestalt of operation of the 6th of this invention. As shown in drawing 18 , the readout circuitry 401 of the gestalt of this operation has the integral means 430 which carries out time quadrature of the current which flows a selection cel, electrical-potential-difference storage means 406A which memorizes the output voltage of the integral means 430, electrical-potential-difference comparison means 408A which compares the size of the output voltage of electrical-potential-difference storage means 406A and said integral means 430, and the control circuit 409 which controls a readout circuitry 401. In drawing 18 , the reference mark with a single equal figure is given to the component which has the same or, same function as drawing 14 the bottom, and the detailed explanation is omitted. The memory cell array 402 of the same configuration as the memory cell array of the gestalt of the 1st - the 4th operation is connected to the input of the integral means 430.
0048 Also in the gestalt of this operation, read-out actuation based on a self-reference method by two read-out by read-out of the 1st and read-out of the 2nd is performed. the reset time Tint1 by the integral means 430 in read-out of the 1st, and the reset time Tint2 in read-out of the 2nd -- a phase -- it is equal. Electrical-potential-difference storage means 406A is memorized until the 2nd read-out actuation ends the output voltage of the integral means 430 outputted at the time of the 1st read-out actuation.

0049 Drawing 19 is the circuit diagram of the integral means 430 of drawing 18 , electrical-potential-difference storage means 406A, and electrical-potential-difference comparison means 408A. The constant current source circuit 431 which branches the current which flows into the integral means 430 is connected to the integral means 430. In the gestalt of this operation, the time constants of the integral means 430 differ in read-out and read-out of the 2nd of the 1st. The time constant of the integral means 430 can be changed by various approaches. First, the time constant of the integral means 430 changes by changing the capacity value of the integral capacitor 432. Also by changing the current Ir which flows in the constant current source circuit 431, the time constant of the integral means 430 can be changed equivalent. How to read to below by changing the time constant of the integral means 430 by making into an example the case where the current Ir which flows in the constant current source circuit 431 in read-out and read-out of the 2nd of the 1st is changed is explained.

0050 If read-out time amount is fixed, as the current Ir which flows in the constant current source circuit 431 will be enlarged, the output Vint of the integral means 430 becomes smaller. output voltage Vint1st(0 of the integral means 430 in case TMR is in "0" storage condition in the current Ir at the time of read-out of the 1st here --) -- In the current Ir at the time of output voltage Vint1st(1) of the integral means 430 in the case of being in "1" storage condition, and read-out of the 2nd The current Ir at the time of read-out of the 2nd is adjusted at the time of read-out of the 1st so that the relational expression of the following TMR may be realized between output voltage Vint2nd(0) and **s of the integral means 430 in the case of being in "0" storage condition.

Vint1st(1)<Vint2nd(0)<Vint1st(0) (2)

0051 Drawing 20 is an explanatory view of operation for explaining actuation of the readout circuitry 401 of drawing 18 . After performing read-out of the 1st to a selection cel, it writes in so that it may be in "0" storage condition, and subsequently, read-out of the 2nd is performed and read-out actuation is performed. First, before going into read-out of the 1st, SUITCHI S3 of drawing 19 is turned on and the integral means 430 is reset. Next, OFF, S4, and S5 are turned on for SUITCHI S3, and read-out of the 1st is started. If the time amount of Tint1 passes, ON, S4, and S5 will be turned off for SUITCHI S3, and the integral means 430 will be reset again. At this time, output voltage Vint1st of the integral means 430 at the time of read-out of the 1st is held at Capacitor Chold (storage). Subsequently, after the writing of "0" storage condition is performed in a selection cel, OFF and S4 are set to ON, S5 is set to OFF for SUITCHI S3, and read-out of the 2nd is started by it. If the time amount of Tint2 (=Tint1) passes, electrical-potential-difference comparison means 408A will compare size with electrical-potential-difference Vint1st currently held at output voltage Vint2nd and Capacitor Chold of the integral means 430, and will judge the storage condition at the time of read-out **a selection cel** of the 1st. Since the current Ir at the time of read-out of the 2nd is adjusted as mentioned above at the time of read-out of the 1st, the following judgment type is materialized clearly.

If it becomes Vint2 nd-Vint1st<0 "0" storage condition If it becomes Vint2 nd-Vint1st>=0 "1" storage condition

0052 In addition, it is possible to write in not "0" storage condition but "1" storage condition after read-out of the 1st as well as the gestalt of the 2nd - the 4th operation. In that case, at the time of read-out **the constant current source circuit 431** of the 1st, the current Ir at the time of read-out of the 2nd is chosen so that the conditions of Vint1st(1) <Vint2nd(1) <Vint1st(0) may be satisfied. The storage condition at the time of read-out **a selection cel** of the 1st is performed based on an above-mentioned judgment type. Finally, if needed, said electrical-potential-difference comparison means 408A outputted and reads, re-writes data in a selection cel, and ends a series of read-out actuation.

0053 In the above explanation, although it is with the time of read-out of the 1st and read-out of the 2nd and the time constant of the integral means 430 was changed equivalent by changing the current Ir of the current source circuit 431, the capacity value of a capacitor 432 may be changed and the time constant of the integral means 430 may be changed as mentioned above, so that a formula (2) may be materialized. Moreover, by read-out and read-out of the 2nd of the 1st, the time constant of the integral means 430 may presuppose that it is fixed, and may set the reset time Tint1 at the time of read-out of the 1st, and the reset time Tint2 at the time of read-out of the 2nd as different time amount in which a formula (2) is materialized. In addition, the integral means 430 also has the effectiveness of removing the offset component of the currents inputted into a readout circuitry, and a noise component from the memory cell array 402.

0054 As explained above, in the readout circuitry 401 of the gestalt of this operation, it has memorized to the capacitor by making the 1st read-out result into the amount of charges. Therefore, digital circuits, such as a register and a judgment means, can also be deleted to the counter for changing into digital value, a reference pulse generation means, and a pan, and a circuit scale can be sharply made smaller than the conventional readout circuitry.

0055 As mentioned above, although this invention was explained based on the gestalt of the suitable operation, the read-out equipment of this invention is not restricted only to the gestalt of operation mentioned above, and performed and reads various change in the range which does not change the summary of the invention in this application, and equipment is also contained in the range of this invention. For example, it is good also as "0" storage condition and a "1" storage condition respectively in the condition that the direction **layer / a pin layer and / free** of magnetization is anti-parallel one and parallel mutually. Moreover, a memory cell array may not be restricted to two-dimensional array, but may be one-dimensional array.

Moreover, like the memory cell from which resistance changes with the electromigration currently indicated by not only TMR but JP,2001-267513,A, even if that from which resistance changes with electric or optical inputs is any, it may be used for a memory cell.

0056

Effect of the Invention As explained above, the readout circuitry concerning this invention makes unnecessary a reference pulse generation means and an integral capacitor, and enables contraction of circuit area or power consumption while it enables low-battery actuation, making digital conversion possible easily and eliminating sneak current and alternating current-noise current from a memory cell array, since VCO is used as an integral means to integrate with the current from a selection memory cell. Moreover, it enables compaction of a read-out rate while not changing the current from a selection memory cell into digital value, and not only a reference pulse generation means but digital circuits', such as a counter's, a register's, and a judgment means', becoming unnecessary and enabling contraction of a circuit scale and power consumption, since the readout circuitry concerning this invention memorizes the current from a selection memory cell as the amount of charges, or an electrical potential difference.

Brief Description of the Drawings

Drawing 1 The circuit block diagram of MRAM used for the gestalt of operation of the 1st of this invention.
Drawing 2 The explanatory view of operation for explaining the pre amplifier of drawing 1 , and actuation of VCO.
Drawing 3 The explanatory view of operation for explaining actuation of the readout circuitry of drawing 1 .
Drawing 4 The circuit diagram of the pre amplifier of drawing 1 .
Drawing 5 The circuit diagram of VCO of drawing 1 .
Drawing 6 TMR resistance-oscillation frequency characteristics in the pre amplifier circuit of drawing 4 , and the VCO circuit of drawing 5 .
Drawing 7 The circuit block diagram of the readout circuitry of the gestalt of operation of the 2nd of this invention.
Drawing 8 The explanatory view of operation for explaining the gain control pre amplifier of drawing 7 , and actuation of VCO.
Drawing 9 The flow chart for explaining actuation of the readout circuitry of drawing 7 .
Drawing 10 The circuit diagram of the gain control pre amplifier of drawing 7 .
Drawing 11 The explanatory view of operation for explaining actuation of the gain control pre amplifier of drawing 10 .
Drawing 12 The circuit diagram of the readout circuitry of the gestalt of operation of the 3rd of this invention.
Drawing 13 The explanatory view of operation for explaining actuation of the readout circuitry of drawing 12 .
Drawing 14 The circuit diagram of the readout circuitry of the gestalt of operation of the 4th of this invention.
Drawing 15 The explanatory view of operation for explaining actuation of the gain control pre amplifier of drawing 14 .
Drawing 16 The explanatory view of operation for explaining actuation of the readout circuitry of drawing 14 .
Drawing 17 some circuit diagrams **(a) of operation explanatory view for explaining and actuation (b)** of the readout circuitry of the gestalt of operation of the 5th of this invention.
Drawing 18 The circuit diagram of the readout circuitry of the gestalt of operation of the 6th of this invention.
Drawing 19 The circuit diagram of the integral means of drawing 18 , an electrical-potential-difference storage means, and an electrical-potential-difference comparison means.
Drawing 20 The explanatory view of operation for explaining actuation of the readout circuitry 401 of drawing 18 .
Drawing 21 The perspective view for explaining the structure and the principle of a tunnel magnetic resistance element.
Drawing 22 the top view **(a)** and sectional view **(b)** for explaining actuation of the memory cell of MRAM.
Drawing 23 The circuit block diagram of MRAM of the conventional example.
Drawing 24 The explanatory view of operation for explaining actuation of the readout circuitry of drawing 23 .
Drawing 25 The flow chart for explaining actuation of the readout circuitry of drawing 23 .

Description of Notations

1, 101, 201, 301, 401, 801 Readout circuitry
2, 102, 202, 302, 402, 802 Memory cell array
3,203 Pre amplifier
4,104,204 VCO
5,105,205,805 Counter
6,106,206 Read-out value register
7 Reference-Value Register
8,108,208,808 Judgment means
9, 109, 209, 309, 409, 809 Control circuit

10,610,710,810 TMR
11,711,811 Word line
12,712,812 Bit line
13 Selection Cel
20 Delay Cel
21 Differential Amplifier
430 830 Integral means
431 Constant Current Source
432 832 Integral capacitor
652 752 Insulator layer
653 753 Pin layer
654 754 Free layer
755 Antiferromagnetic Substance Layer
756 Cap Layer
833 Charge Amp
834 Reference Pulse Generation Means
10a TMR of a selection cel
11a Selection word line
12a Subdevice-bit line
103A, 303A Gain control pre amplifier
306A, 406A Electrical-potential-difference storage means
308A, 408A, 808A Electrical-potential-difference comparison means
807A Presetting register
C, Chold Capacitor
S1, S2, S3, S4, S5 Switch

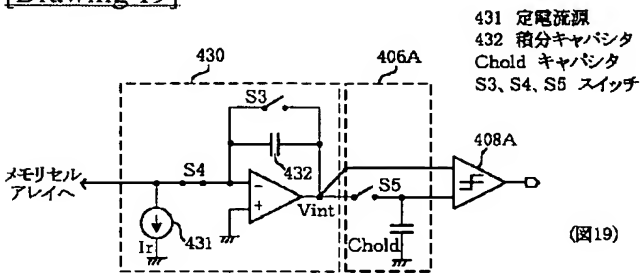
* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

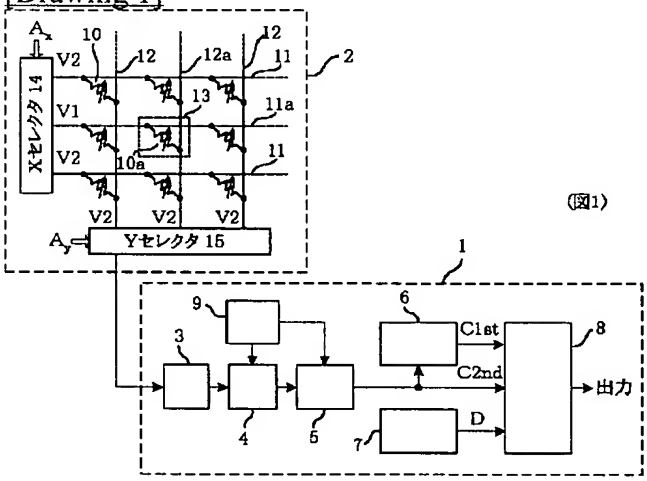
DRAWINGS

[Drawing 19]



(図19)

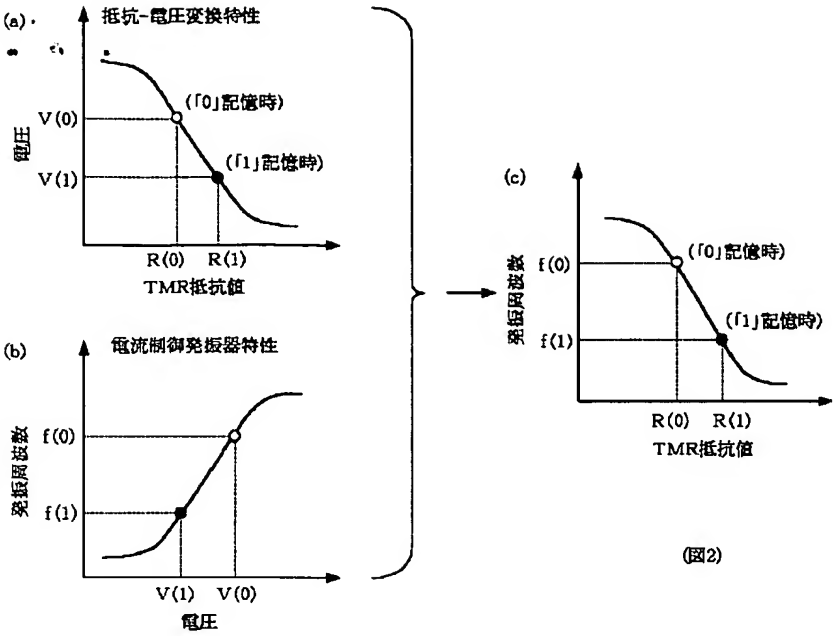
[Drawing 1]



(図1)

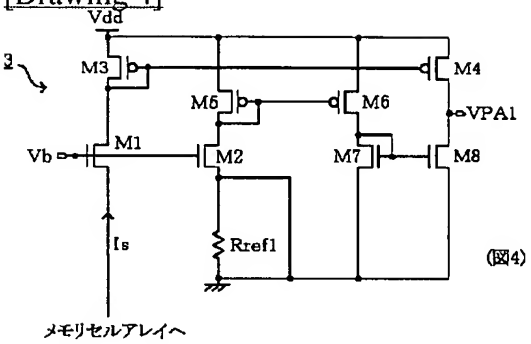
1 読み出し回路	6 読み出し値レジスタ	10a 選択セルのTMR
2 メモリセルアレイ	7 基準値レジスタ	11 ワード線
3 プリアンプ	8 判定手段	11a 選択ワード線
4 VCO	9 制御回路	12 ビット線
5 カウンタ	10 TMR	12a 選択ビット線
		13 選択セル

[Drawing 2]



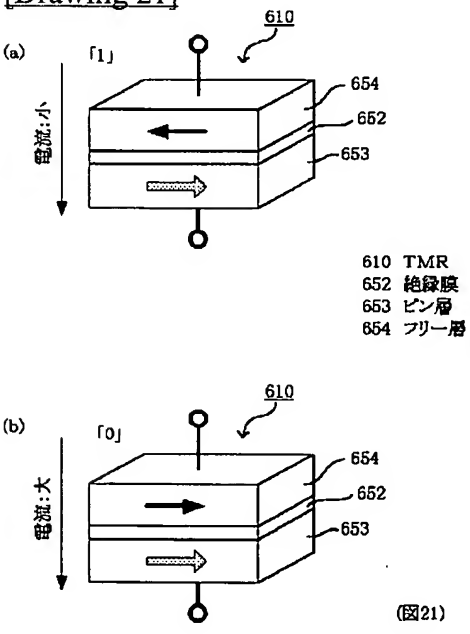
(図2)

[Drawing 4]



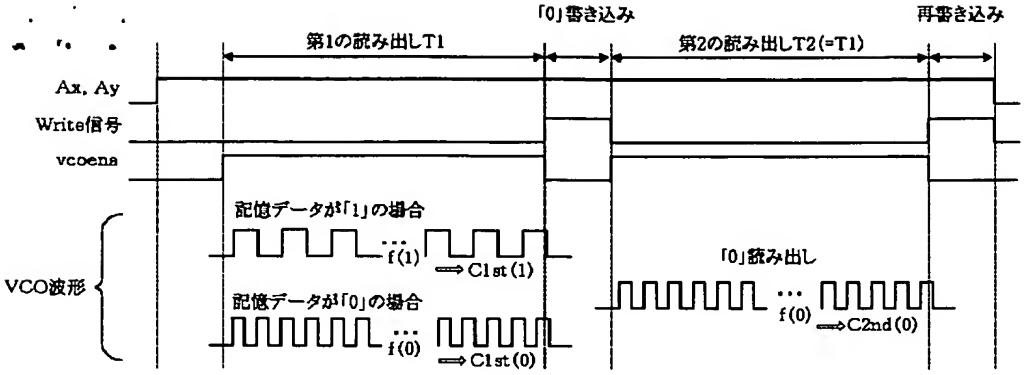
(図4)

[Drawing 21]



(図21)

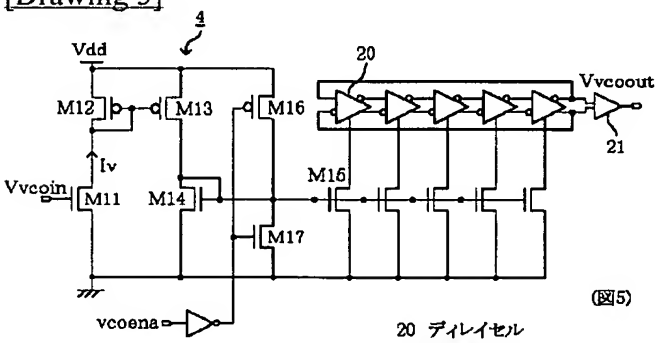
[Drawing 3]



C2nd-C1st-D<0⟹「0」を出力
C2nd-C1st-D≧0⟹「1」を出力

(図3)

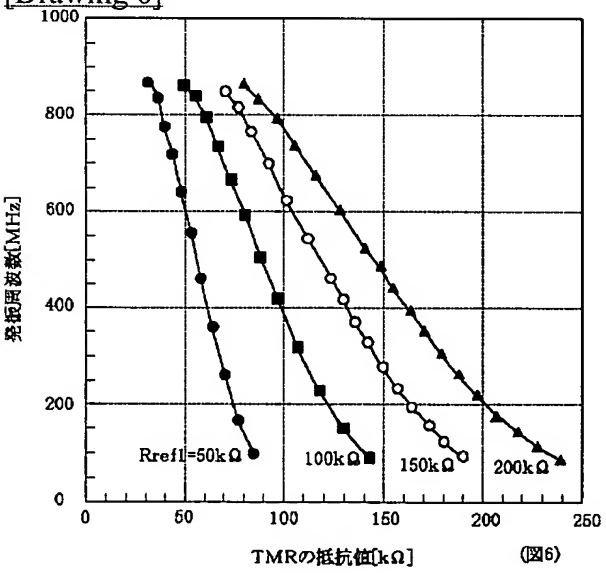
[Drawing 5]



(図5)

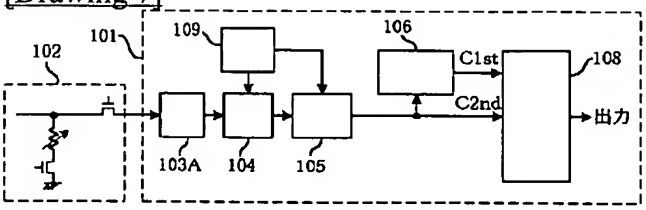
20 ディレイセル
21 差動アンプ

[Drawing 6]



(図6)

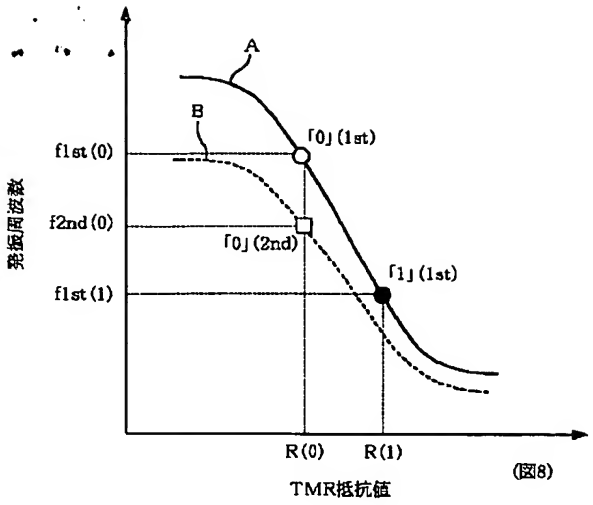
[Drawing 7]



(図7)

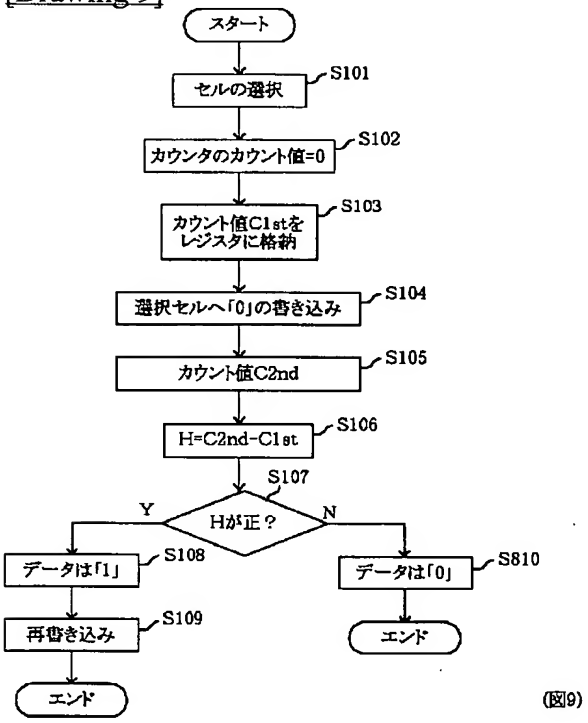
101 読み出し回路
102 メモリセルアレイ
103A ゲインコントロールプリアンプ
104 VCO
105 カウンタ
106 読み出し値レジスタ
108 判定手段
109 制御回路

[Drawing 8]



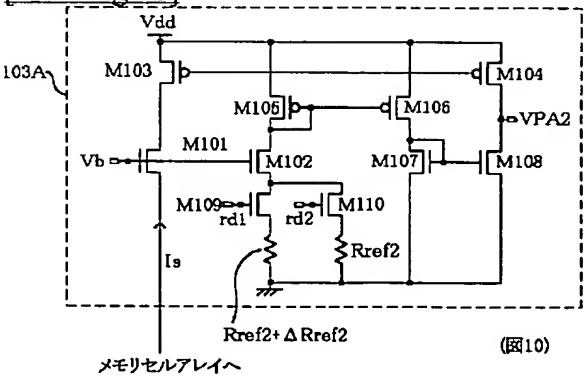
(図8)

[Drawing 9]



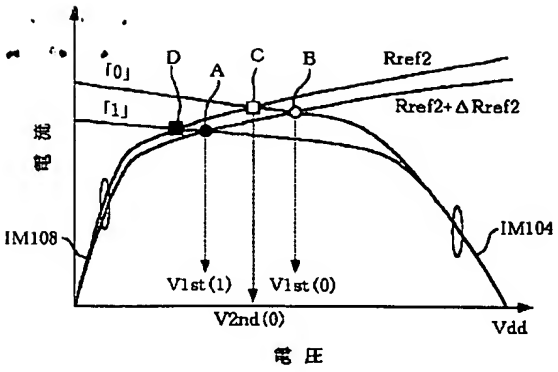
(図9)

[Drawing 10]



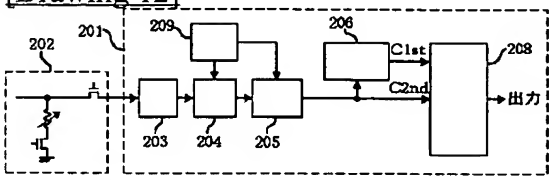
(図10)

[Drawing 11]



(図11)

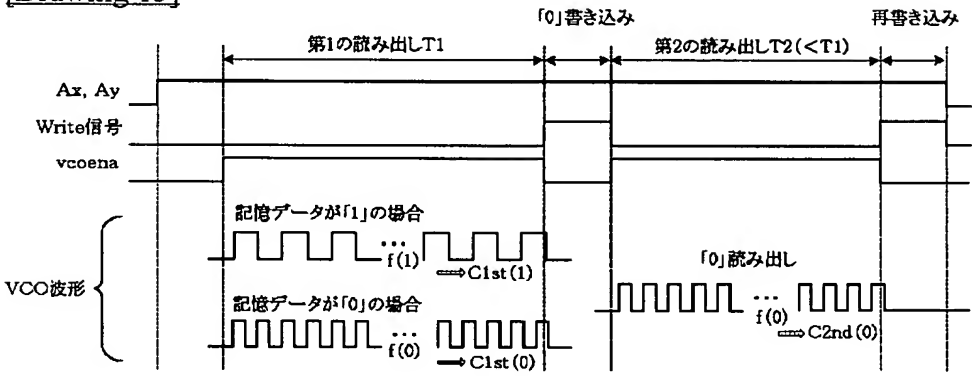
[Drawing 12]



201 読み出し回路
202 メモリセルアレイ
203 プリアンプ
204 VCO
205 カウンタ
206 読み出し値レジスタ
208 判定手段
209 制御回路

(図12)

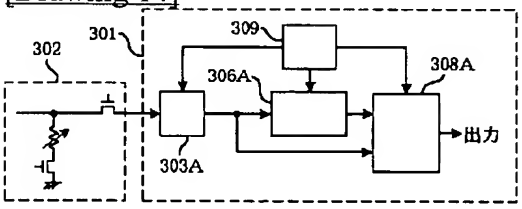
[Drawing 13]



C2nd-C1st<0⟹「0」を出力
C2nd-C1st≧0⟹「1」を出力

(図13)

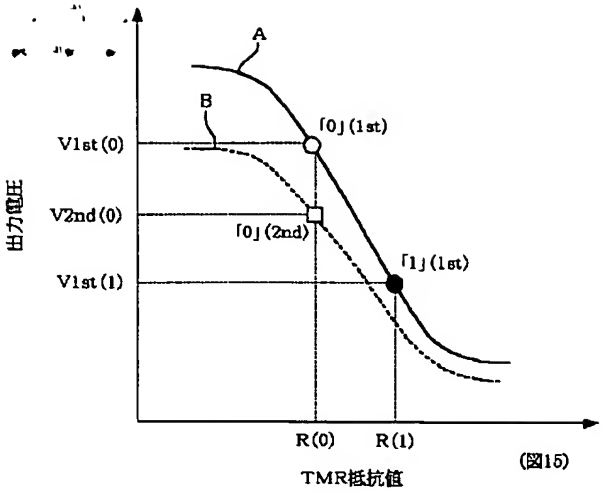
[Drawing 14]



(図14)

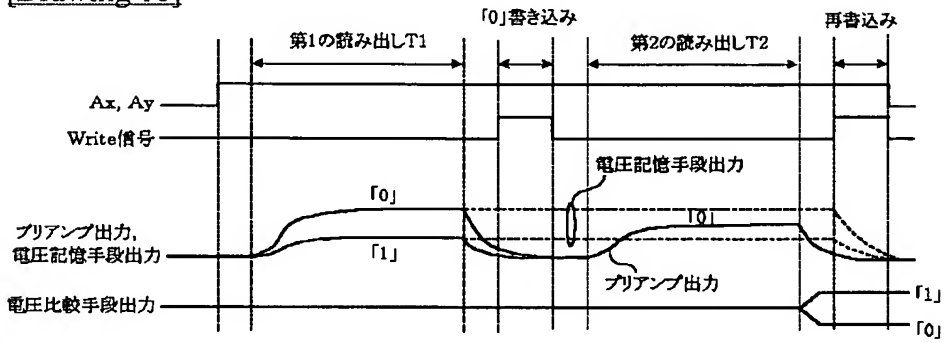
301 読み出し回路
302 メモリセルアレイ
303A ゲインコントロールプリアンプ
306A 電圧記憶手段
308A 電圧比較手段
309 制御回路

[Drawing 15]



(図15)

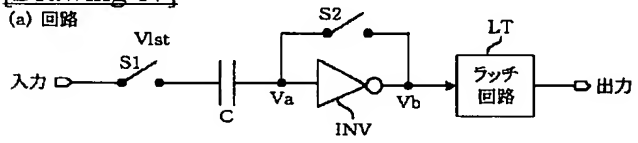
[Drawing 16]



(図16)

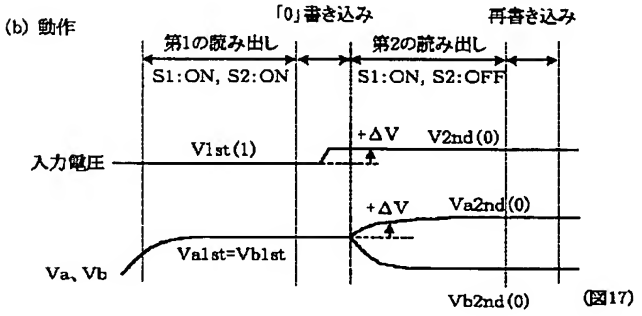
[Drawing 17]

(a) 回路



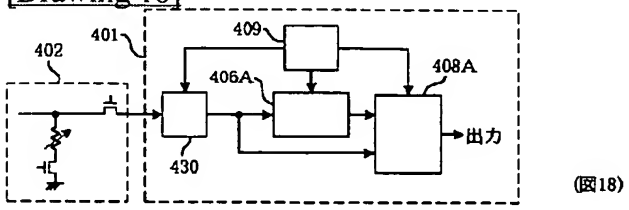
C キャパシタ
S1、S2 スイッチ

(b) 動作



(図17)

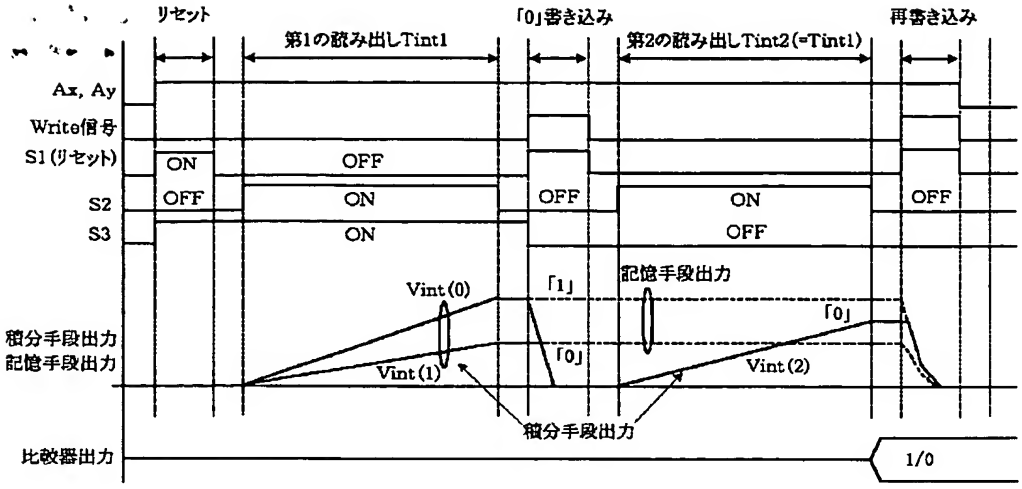
[Drawing 18]



(図18)

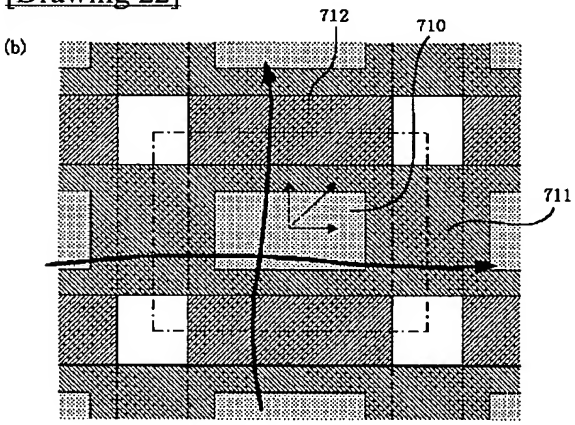
401 読み出し回路
402 メモリセルアレイ
430 積分手段
406A 電圧記憶手段
408A 電圧比較手段
409 制御回路

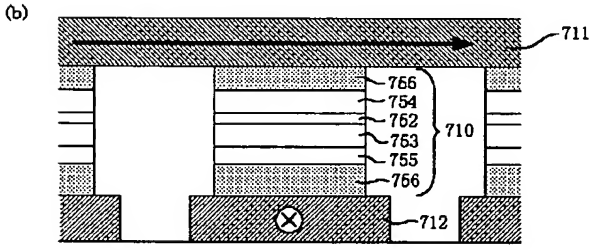
[Drawing 20]



(図20)

[Drawing 22]

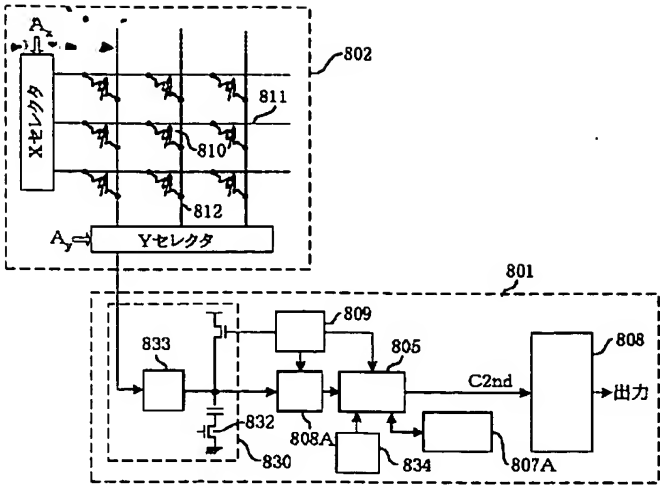




(図22)

710 TMR
711 ワード線
712 ビット線
752 絶縁膜
753 ピン層
754 フリー層
756 反強磁性体層
756 キャップ層

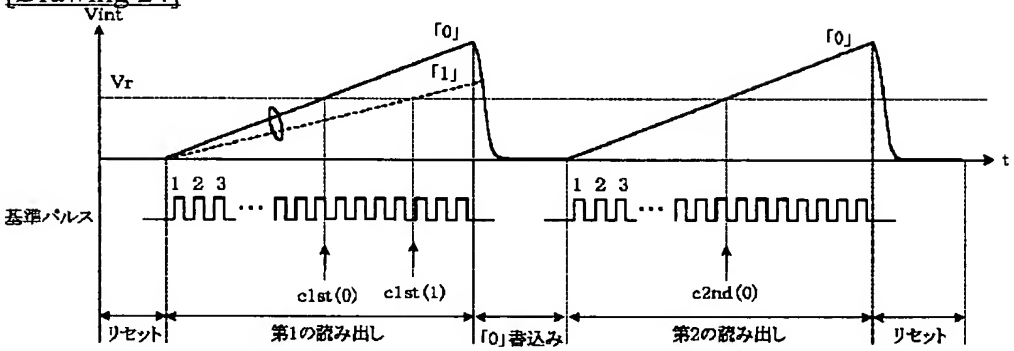
[Drawing 23]



801 読み出し回路
802 メモリセルアレイ
805 カウンタ
807A プリセットレジスタ
808 判定手段
808A電圧比較手段
809 制御回路
810 TMR
811 ワード線
812 ビット線
830 積分手段
832 積分キャパシタ
833 チャージアンプ
834 基準パルス生成手段

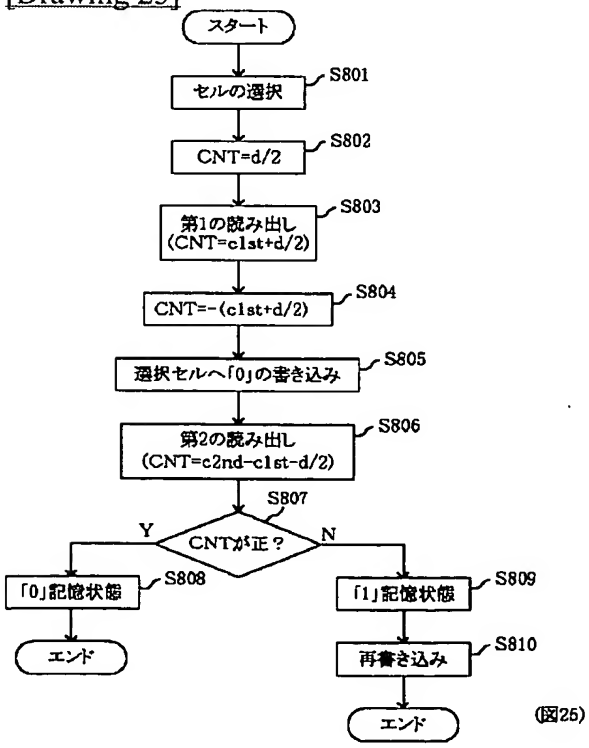
(図23)

[Drawing 24]



(図24)

[Drawing 25]



(図25)